RAL

DESIGN & DISCOVERY

Open Days July 1990

RUTHERFORD APPLETON LABORATORY

SCIENCE AND ENGINEERING RESEARCH COUNCIL

INTEGRATED CIRCUIT DESIGN AND TEST

Rutherford Appleton Laboratory Electronics Division has 25 people engaged on IC (Integrated Circuit) Design, Test and the support of IC Computer Aided Design in the broader academic research community. In addition to the general support provided, ICs (chips) are designed and used in projects and experiments which pursue leading-edge scientific and engineering endeavour across the whole range of SERC's remit. This in-house design activity is carried out in close collaboration with the electronic systems designers who are responsible for these programmes. The chips are then produced using advanced commercial foundry services and brought back to RAL for testing prior to their incorporation into working systems. In this way, the facilities provided to the academic community are thoroughly tested and thus the whole community benefits.

In addition to the design and test activities, the Division is also responsible for providing CAD support to academic researchers who wish to design their own chips. This involves the support of hardware and software for CAD as well as providing direct assistance and training to the researchers.

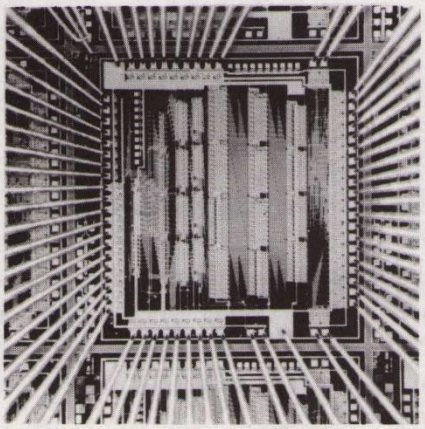
Layout

RAL is involved with many european collaborations, through which the Electronics Division will be providing similar services to european Universities and to Industry. Integrated Circuits designed at RAL are used in experiments at a number of leading laboratories around the world. Their applications include particle physics, space science, robotics, medical electronics and communications.

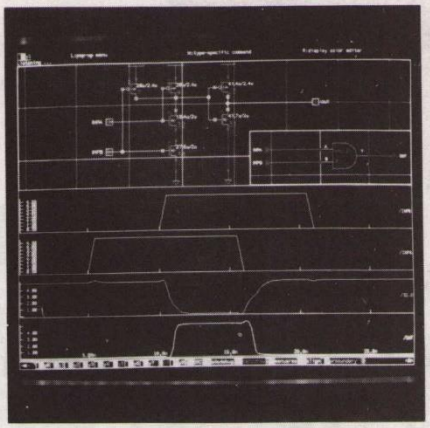
The wide variety of design and fabrication skills available ensure that the best possible solution can be found for each requirement. Each technological option(eg. Silicon CMOS or Bipolar, Gallium Arsenide) has particular properties which can be exploited to meet certain needs. Some typical parameters that need to be considered when selecting the best technological option are: whether information is processed in analogue or digital form; the speed of operation; power consumption; signal and noise levels; radiation hardness; packaging; quantities required and cost.

For high performance, full custom design is required to take maximum advantage of the process capabilities. Where the demands are not so great, a standard cell approach can be used: rows of cells are pre-designed and may be interconnected in a variety of ways to obtain different circuit configurations at lower cost. Less critical circuits can be realised using Gate Arrays which offer an even cheaper alternative and a fast turnround.

As a precursor to these design processes, it is necessary to consider the basic hierarchy of the circuit and capture the components in a computerised form. Detailed layout is then performed with the latest CAD tools in order to produce a completed design in a form that can be sent to the chip manufacturer.



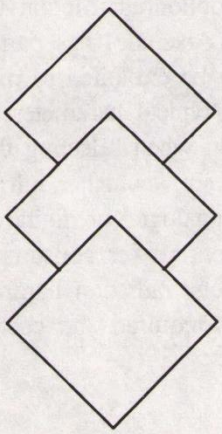
Test



Simulation

Before finalising the design, digital circuits require extensive simulation to ensure that they will perform the correct function with the required speed. Similarly, analogue circuits must be characterised for gain; frequency response; noise; power dissipation; and sensitivity to component value spread, temperature and power supply variation. Once a design is sent for fabrication, errors cannot be corrected.

When silicon wafers are processed, it is usual that only a certain proportion of the chips on them will be working circuits(the 'yield'). It is necessary to test the chips on the wafer and pick out the good ones. Wafers and packaged chips are tested at RAL using modern semi-automatic test equipment, to ensure that the whole design and manufacturing cycle has been successfully completed and that the chips meet the original specification.



For further information , please call either Peter Sharp or Andrew Kurzfeld(0235 446242 or 0235 445286).

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